REMARKS

In the Office Action dated September 3, 2003, the Examiner has rejected claims 1, 3-8, 12, 13, and 17 under 35 USC 102(a) as anticipated by Walker (U.S. Patent No. 6,275,277), rejected claims 1-5, 9, 12, 14, and 17 under 35 USC 102(e) as anticipated by Hasegawa (U.S. Publication 2003/0038343), rejected claims 10 and 15 under 35 USC 103 as unpatentable over Walker in view of Ueta (U.S. Patent 6,590,919), rejected claims 10 and 15 under 35 USC 103 as unpatentable over Hasegawa in view of Ueta, rejected claims 11 and 16 under 35 USC 103 as unpatentable over Walker in view of Hahn (U.S. Patent 6,131,880), and rejected claims 11 and 16 under 35 USC 103 as unpatentable over Hasegawa in view of Hahn. In response thereto, the applicants have amended claims 1, 5 and 9 and cancelled claim 4. Claims 1-3 and 5-17 remain at issue.

Walker teaches the dicing of a wafer by imaging registration marks used for alignment. Specifically, Figure 20 and column 13 lines 12 through 19 of Walker teaches:

> When the assembly is mounted on the vacuum chuck to cut wafer 115 (i.e., circuitry patterned side 117 of wafer 115 is face down) scribe marks 240 and 245 in transmissive substrate 100 are visible through glass material 102 and may be used for alignment. The camera uses alignment or registration marks 240 and 245 to cut wafer 115 from the backside, since marks 240 and 245 are relative to micro display area 155 of wafer 115.

Hesegawa teaches the dicing of a wafer by recognizing certain features on the wafer such as electrode pads and metal wire pads. Once the features are identified, the location of the scribe lines are determined by their positions relative to the recognized features. Specifically, paragraphs [0110] and [0111] of Hesegawa provide:

> [0110] As shown in FIG. 12(D), pattern shapes of a plurality of electrode pads 301 or metal wiring layers 303 formed on the surface 109 side of the semiconductor wafer are first recognized from the back of the semiconductor wafer 1101 by the infrared camera 1211. Consequently the scribe areas 1103, which exist on the surface 109 of the semiconductor wafer 1101, are recognized by the dicing device.
>
> [0111] Next, the second blade is placed on the center line of each scribe area 1103. Thereafter, the back 105 of the semiconductor wafer 1101 is ground (half-cut) about 25 .mu.m by the second blade so that each steplike section 107 is formed (see FIG. 13).

Neither Walker or Hesegawa, either separately or in combination, teach the dicing of a wafer by generating a picture of the wafer, mapping the scribe lines on the wafer from the picture, and then providing the coordinates of the scribe lines to a dicing machine. In contrast, Walker performs wafer dicing by imaging registration marks for alignment. Hesegawa performs dicing by determining the location of scribe lines relative to imaged features on the wafer, such as electrode pads and metal lines.

The applicants therefore submit that claim 1 is allowable. Although patentable in their own right, claims 2, 3 and 5-11 are allowable based on their dependency on claim 1.

Claims 12-17 are allowable for essentially the same reasons as provided above with regard to claim 1.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

James W. Rose
Reg. No. 34,239

P.O. Box 778
Berkeley, CA 94704-0778
(650) 961-8300